2814
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Docket No.: GR 98 P 1379 D

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By: _____ Date: 11/5/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Lars-Peter Heineck et al.
Applic. No.	:	09/885,553
Filed	:	June 20, 2001
Title	:	MOS Transistor in a Single-Transistor Memory Cell Having a Locally Thickened Gate Oxide
Art Unit	:	2814

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

Japanese Patent Abstract JP 06 283 686 (Ota), dated October 7, 1994;

Japanese Patent Abstract JP 9 186 250 A2 (Ryu), dated July 15, 1997;

Kurimoto, K. et al.: A T-gate Overlapped LDD Device with High Circuit Performance and High Reliability", International Electron Devices Meeting 1991, Washington, D.C., December 8-11, 1991, pp. 541-544, XP-000342187.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications,

patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

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For Applicants

Date: November 5, 2001

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